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Sheet 1 of 2

Complete If Known

Application Number	10/637,408
Filing Date	August 7, 2003
First Named Inventor	Sachin G. Deshpande
Group Art Unit	
Examiner Name	
Attorney Docket Number	SLA1306

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
KV	U1	US-6,118,784	09/12/2000	Tsuchiya et al.	
KV	U2	US-2002/0136237	09/26/2002	Tsuchiya et al.	
KV	U3	US-2002/0136216	09/26/2002	Tsuchiya et al.	
KV	U4	US-2002/0024960	02/28/2002	Tsuchiya et al.	
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KV	U6	US-2002/0021705	02/21/2002	Tsuchiya et al.	
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KV	F1	WIPO - WO 02/073933	09/19/2002	British Telecommunications		
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KV	F3	WIPO - WO 01/69887	09/20/2001	SRI International		
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
KV	O1	"Transition Mechanisms for IPv6 Hosts and Routers," R. Gilligan, pp. 1-26, August 2000.	
KV	O1	"Dual Stack Hosts Using "Bump-in-the-API" (BIA)," Seungyun Lee et al., pp. 1-14, April 2002.	
KV	O2	"Dual Stack Hosts Using "Bump-in-the Stack" Technique (BIS)," K. Tsuchiya et al., pp. 1-12, February 2000.	
KV	O3	"Stateless IP/ICMP Translation Algorithm (SIIT)," E. Nordmark, pp. 1-23, February 2000.	
KV	O4	"IPv4-IPv6 Dual Stack Hosts Using the "Bump-In-the-Stack" Technique (BIS)," Yoshifumi Atarashi et al., IEICE Trans Commun., Vol. E84-B, No. 8, pp. 1996-2000, August 2001.	
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/Kacy Verdi/

01/05/2007